So what happened this year at SPIE AL?

Part I: Data

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The 2019 SPIE Advanced Lithography EUVL Conference was held at the end of February in San Jose, CA. I am late this year on my reporting due to extensive travel in March. Here are highlights and details on the status of EUVL. I will present data in this blog, and invite you to read my next blog, where I will discuss my further thoughts on the data and present current and future challenges of EUVL.

Highlights

This year, many of the papers can be described as dedicated to improving yield in coming nodes of 5 nm and beyond, as EUVL technology to support the 7 nm node seems to be ready, and any remaining challenges in fabs today are mostly out of the sphere of conference discussions. The main challenges for 7 nm nodes involve scanner uptime, and the focus is now on EUVL infrastructure apart from scanner.

EUVL Scanner

EUVL scanner is now maturing and at 0.33 NA will continue to deliver higher throughput, mainly via increases in source power. In the second half of 2019, scanners NXE3400C with 170 wafers per hour (WPH) will be available. It is important to note that advertised throughputs are for 20 mJ resists while actual resist dose is 50-70 mJ, meaning a smaller throughput. High NA scanners for the 3 nm node are targeted for 2023 with 185 WPH. EUVL scanners are now ready, hence this year the room was not crowded during ASML's scanner update – while in previous years there was standing room only during these presentations.

This version of scanner will have a modular design to improve mean time to repair (MTTR), which will improve its uptime –the main issue with the EUVL scanner today. Although 30 scanners are planned to be shipped this year, only about five will be the new NXE3400C. Scanner is approaching a target of <1 defects per 10,000 passes. A question was asked about the composition of defects so that source can be further determined, and this question was well answered in a paper by Vadim Banine of ASML. He showed how a 100x reduction in added defectivity has been achieved in the last two years. Further improvement is planned

via improving part cleanliness, minimizing plasma forces and tailoring crossflows to counter electric/plasma transport forces. Uptime for NXE3400B is still ~75% with a target of 90%. Although uptime is expected to increase with improvements of <8 hours for collector swap and in-line fill system for tin.

EUV Source

Source power is now >250 W and 99.99% stable. The increase in source uptime has been coming through an increase in collector lifetime (data for 0.1% loss per gigapulses shown), higher droplet generator lifetime (>1000 hours) and in-line filling of tin, which will require no downtime for droplet generator. Source uptime is now >80% and there is a plan for >90% by 2020. Currently 1/3 of downtime comes from droplet generators. Collector lifetime now is <0.1% loss per gigapulse, with plans to make that 0.03% per gigapulse. This is a significant improvement. Cymer, now part of ASML, has a path toward 500 W. I am not yet clear on how far Sn LPP can be extended beyond 500 W, which may be needed for a high NA tool to keep up the high throughput.

Gigaphoton, the second supplier for EUV sources, also continues to make progress. They are currently at 125 W with 10 kW CO_2 lasers, and plan for 330 W with >6% CE via improvement of beam uniformity at plasma, plasma parameter optimization via measurements and upgrade of CO_2 lasers.

Metrology sources are still maturing and are needed for mask defect inspection tools. Zeiss claimed that they have a source that meets HVM requirements for AIMS. There was a new design presented for Sn LPP metrology source by ISTEQ.

Mask and Pellicle Update

The main near term challenge for masks is the development of thinner absorber layer with an alternate material for EUV Mask. Once the material is chosen, we will also need to understand the properties of new mask absorbers for OPC. Veeco reported that they can successfully etch Ni and Co via ion beam etch (IBE), with an end point control system and side wall angle control.

AMTC can now get 5 nm placement accuracy on masks. Chris Progler of Photronics gave examples on how mask can help reduce stochastics type defects. Yamane of EIDEC showed that there was no significance influence of mask LWR on LCDU or defect printability. ASML showed that EPE can be reduced by using thinner high-K absorbers.

The lack of patterned mask defect inspection tool is being addressed by companies via wafer inspection or some internal ad hoc solution for the 7 nm node. Lasertec and KT are working on this tool, but I did not see any update. Lasertec is trying to be the first in this market as KT has waited. I wish both of them good luck as competition is a good thing for the industry. In the absence of APMI tools, alternate lensless techniques are also being developed for mask inspection, as reported by PSI.

Mask pellicle now has >83% transmission with <0.04% reflectivity. However, Samsung and TSMC are not using pellicles in their scanners at the 7 nm node. We may get to required transmission of 90% but progress on that front has been slow and one may have to go with slightly less value by taking a small hit in throughput, if a decision is made to use pellicles.

Resist

I heard that CAR is now ready to support EUVL at the 7 nm node, but new resists are needed at future nodes to meet the requirements of dose, sensitivity, LER and defectivity. Several new chemistries are being investigated. Lots of fundamental work with new chemistries was reported, but I have not yet seen a clear roadmap of open questions and how and when we will get answers. Only thing that is clear is that EUV resist chemistry is dominated by secondary electrons, and we need to learn more about it.

Stochastics

There were quite a few papers delivering solutions for tweaking the process window, made narrow by defects caused by stochastics, and in a year IMEC has made a good advance in understanding the defectivity that is driven by stochastics. In order to continue this study, we need more sensitive broad-band plasma-based metrology for detection of not -OK (NOK) beyond the limit of 1E-12. Several solutions were proposed for creating a larger process window in the presence of defectivity coming from stochastics: Coatings can be used to improve the defect metrology detection (IBM), data from RGA can be used to reduce defectivity (IMEC), and sequential infiltration synthesis (SIS) was shown by IMEC to reduce nano-breaks by 2x, expand process window and improve CDU by 20-30%. It was pointed out that dark area needs to be carefully considered in understanding defectivity, as material is also contributing to stochastics. It looks like the source of microbridge floor seems to be more than photon shot noise, and material stochastics is equally important.

It is now clear that the classic process window does not tell us about process robustness, as rare events (stochastics defects) are described by tales of distribution. Mark Moslow of IMEC had interesting results by fitting the tales of distribution via higher moments.

LAM mentioned that there is an industry wide need for physical and chemical characterization capability of stochastics related defects. TEL showed that resist deposition and development steps can be

tuned to reduce bridging defects. In short, there is significant work being done to figure out how to create a process window at the 7 nm node, but we need to increase our understanding to continue to have success at the 5 nm node and beyond.

Patterning

Collaboration of design, process and materials will be needed in future nodes to achieve required patterning. Although conference papers from suppliers and consortia focused on topics which will improve yield, none were from chip makers.

EUV double patterning (EUV DP) was proposed for metal layers and 20 nm isolated features were printed with 298 mJ CAR resist with LER of 2.9 nm. Also, beyond the 7 nm node, EUV SRAFs will be needed.

Mask OPC is more complex for EUV and not simpler, as it was previously assumed. More EUV is coming to front-end via nanosheet gates and bright field imaging for metals, and it will happen at 0.33 NA. EUV hybrid double patterning and cuts will be needed to mitigate stochastics defects and improve LCDU.

Additional Highlights

Future is Quantum, Dario Gill (IBM)

Manufacturing Challenges for Quantum Computers (QC): Main thing now is not how many qubits one has, but how to keep the decoherence at bay. We don't fully understand all the reasons for decoherence. 100 nm is the minimum feature size (Josephson Junction) and reduction of size is not the key right now (or foresee a roadmap similar to Moore's Law, where smaller is better). Materials, packaging and manufacturing challenges are there for various versions of QC, but the information is not public. Quantum computers can be ready from 2020+ to 2050 time frame (which I took to mean at least not for another decade). Three pillars of information processing will emerge in the future – precise manufacturing, AI, and biological and quantum computers. Hence, what we do best in semiconductor manufacturing or precise manufacturing will always fullfill a need.

NAND is going 3D and will use EUVL. 512 layers are now planned. Multifocal imaging (MFI) and source mask optimization (SMO) will be required for NAND. NAND scaling will require EUV. (Jeogdong Choe, Tech Insight)

Best Papers

I found the following four papers to be very interesting, with valuable information:

- *Future is Quantum*. A very nice overview of Quantum Computers (plenary talk, Dario Gill, IBM)
- *EUVL Insertion into Logic*, a clear outline of how EUVL will be used, challenges and status (Keynote talk, Ryoung-Han Kim, IMEC)
- *EUVL: the Natural Evolution of Optical Microlithography* – a very engaging presentation (Keynote talk, Bernd Geh, Carl Zeiss)
- *Advanced Particle Control in EUV Scanners* – a definitive overview of the contamination issue and approaches to addressing it in the EUVL scanner (Session 9, Vadim Banine et al, ASML)

Best Paper Format

Two speaker presentations by ASML and LAM – Patterning in the Stressful World of 3D NAND (fresh new approach)

Speed presentation for selected poster papers (nice overview).

Best Animation

How ASML (Martin- yep, it is still a one man company) got Carl Zeiss to make quick progress on optics.

New Words /Acronyms heard

- k4 to define local CD uniformity (LCDU). LCDU = k4(1/NILS). Sqrt(h.nu/dose) [Bernd Geh, Carl Zeiss]
- XLD – extremely long downtimes [ASML, which plans to reduce them from currently >24hhours to zero]
- DTCO – design technology co-optimization, which denotes that we are now moving from litho-driven scaling to litho- and design-driven scaling.
- STCO – system technology co-optimization, an alternate term for
- Bananicity [used by Bernd Geh to describe certain aberrations]

Best Quotations

- "You are thinking too classically." (Mentioned by Dario Gill as a saying in his group – IBM- Q)
- "You can only make what you can measure." (Bernd Geh, Carl Zeiss)
- "If an 'old' lithographer (someone age 60 or older) tells you that something is right, he is right. Listen to him carefully. If he tells you something will not work, turn other way and RUN." (Bernd Geh, Carl Zeiss)
- "k1 became a simple measure on how well we can push the limits of physics." (Bernd Geh, Carl Zeiss)